independent cell networks (12, 13; 22, 23; 32, 33) while at least said cell of the integrated circuit to be tested is in test mode.

8. (amended) The method of claim 4, comprising the additional step:

suppressing leakage currents in said circuit cell by turning off one or more of said control means while said circuit cell is in standby mode.

11. (amended) The integrated circuit of claim 9, comprising control circuitry (14, 15; 24, 25; 34, 35) to deactivate said p- and n-channel transistor networks (12, 13; 22, 23; 32, 33) or to electrically separate them from each other, and wherein said control circuitry is connected in series with said n- and p-channel transistor networks.

12. (amended) The integrated circuit of claim 10, further comprising load means (16, 17; 26, 27; 36, 37) which act as loads for said p- and n-channel transistor networks while said network (12, 13; 22, 23; 32, 33) is in test mode.

13. (amended) The integrated circuit of claim 10, comprising connection circuitry (38, 39) connecting electrical signals of the control circuitry (34, 35) to other subcircuits for the purpose of